A Digital Array Radar with a Hierarchical System Architecture

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***Abstract* — A digital array radar system prototype is presented that makes use of a hierarchical digital backend coupled with highly-integrated, multi-channel RF transceivers. The general benefits of using such a hierarchical architecture are briefly discussed, along with how this prototype is in line with a vision for future radars that fully embrace the concept of low-cost integration in a panelized platform. A target tracking example is given using the prototype that illustrates some specific advantages to using a hierarchical digital backend.**

***Index Terms* — Data management, distributed computing, phased array radar, radar data processing, radar tracking.**

I. Introduction

Next-generation radar systems must meet practical levels of cost, size, and weight while providing more flexibility and functionality at the system level [1]. At the same time, the same systems must satisfy increasingly stringent demands on prime power, noise figure, and linearity. These engineering challenges are being met by a move toward active arrays with efficient RF frontends, improvements in packaging and integration, and increasing the role of digital electronics by pushing them closer to the aperture of the system. Digital backends provide levels of flexibility and functionality that simply cannot be achieved using older methods; multiple receive beams with high dynamic range [2], adaptive jammer suppression, and multifunction radar [3] are all enabled by digitization. The tradeoff in the design is an increased functionality provided by having digitization at every element versus the amount of data that must be handled and processed. Intelligent use of a hierarchical digital architecture with distributed processing capability eases the data flow requirements without limiting radar system functionality. High levels of RF integration are possible by using direct conversion on-chip receivers, which eliminate the IF components and allow for less than one transceiver IC per element through the use of multi-transceiver ICs. This level of integration promises to increase the availability of phased arrays by driving down the cost substantially.

In this paper we present a digital array radar prototype based on a panelized and highly-integrated RF platform that utilizes a hierarchical digital backend in order to provide full radar functionality without excessive host PC interaction. Various benefits of the hierarchical digital backend with full element-level control, as implemented in the prototype, are demonstrated through an example of full radar functionality wherein an indoor target is tracked using a single-panel, monopulse comparison tracking algorithm.

II. DAR Prototype System

A. RF System Overview

The digital array radar (DAR) 16-element prototype is shown in Fig. 1. The methodology in designing this prototype was to provide a viable demonstration of what a future, advanced, highly integrated digital array radar may be like. As the digital portions of radar systems move closer and closer to the antennas, the traditional, multiple IF transceivers will likely be replaced by more integrated solutions, such as direct-conversion transceivers or even advanced, ultra-wide-band, direct RF sampling systems. Cost, packaging requirements, and the total chip count per element are drastically reduced with the elimination of IF components and/or the integration of multiple transcievers onto individual ICs. An example of this level of integration is a recent demonstration of a 6-18 GHz, 8-element phased-array receiver chip with an analog beamformer on a 2.2mm x 2.3 mm die [4]. Furthermore, panelization of radar subarrays through the use of standard surface mount, "motherboard-like" technology allows reductions in both cost and complexity over ceramic or metal-based packaging.

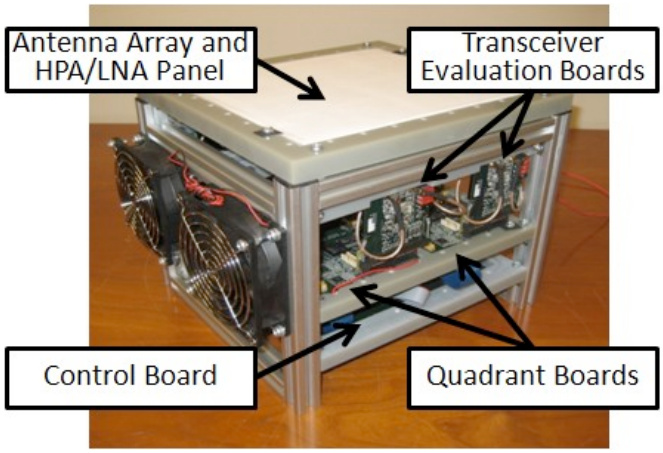

Fig. 1. The full DAR prototype system

It is with these considerations in mind that we chose to integrate a set of direct-conversion SiGe WiMax transceiver ICs from Sierra Monolithics, Inc. into a panelized digital backend for the prototype. These ICs offer two T/R channels at S band (3.1-3.5 GHz) with extensive programmability at both RF and baseband. In this respect, they represent an example of a highly-integrated, commercial product with the potential to provide

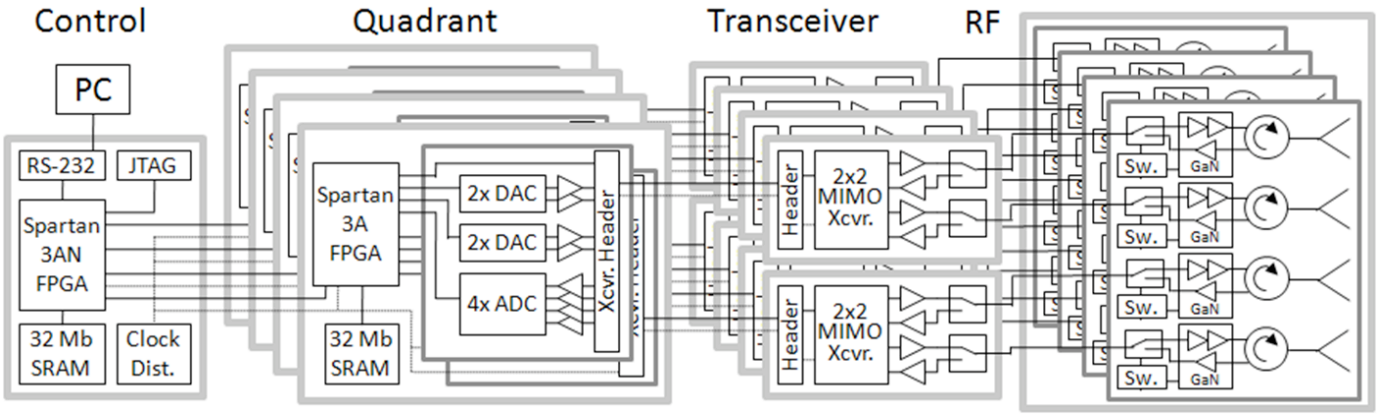

Fig. 2. DAR prototype system block diagram, showing the RF frontend, transceivers, and digital backend

future radar systems with a very low chip count per element. The overall system block diagram is shown in Fig. 2. A separate RF panel, which connects to the baseband/digital backend panel through the transceivers, consists of a multilayer Rogers 4350 PCB with an integrated aperture-coupled, stacked patch antenna array, the design of which is discussed in [5]. To provide for high-power applications, a version of this panel with plastic-packaged, highly efficient GaN HPA/LNA MMICs with air cooling is currently being created to demonstrate such a system's capability to meet next-generation power, cost, and efficiency requirements, but it was not used for the indoor demonstrations in this paper.

B. Hierarchical Digital Backend Implementation

In choosing an architecture to implement for the digital backend, several issues were considered. In order to support digitization at each element, a system must be designed to intelligently move and process the large amount of data that is generated. The simplest digital backend architecture is one in which there is a single processing node to which all elements in the array are connected (Fig. 3a). The processing requirements of this node scale with the number of elements, and eventually it becomes impractical to implement this node as a single processing unit. A hierarchical design (Fig. 3b), such as the one in [6], avoids this problem by fixing communication and processing requirements of each node as the array scales. The communication overhead associated with this is on the order of the logarithm of the number of elements, but it enables the use of computational and I/O resources with significantly reduced complexity, more practical performance levels, and an order of magnitude lower cost.

The DAR prototype exploits this fact by using a two-level hierarchy (see Fig. 2) made up of five small FPGA—four "quadrant" FPGAs and a central "control" FPGA—instead of a single FPGA of considerably more complexity and size. Each quadrant FPGA drives the ADCs, DACs, and transceivers, processes and stores element data, and communicates with the control FPGA. For the prototype, 12-bit, multi-channel ADCs and DACs were used, operating at 24 MSPS, which is in line with the maximum baseband frequency of the SiGe transceivers of 7 MHz for this generation. The system is cycle-synchronous through the extensive use of digital clock managers, and a 40 MHz LO reference is distributed to each transceiver board by a clock distribution circuit. Both the control and quadrant FPGAs have microprocessors running at 24 MHz that interface with the rest of the FPGA hardware, and the control FPGA interfaces to a host PC running a GUI-based MATLAB program.

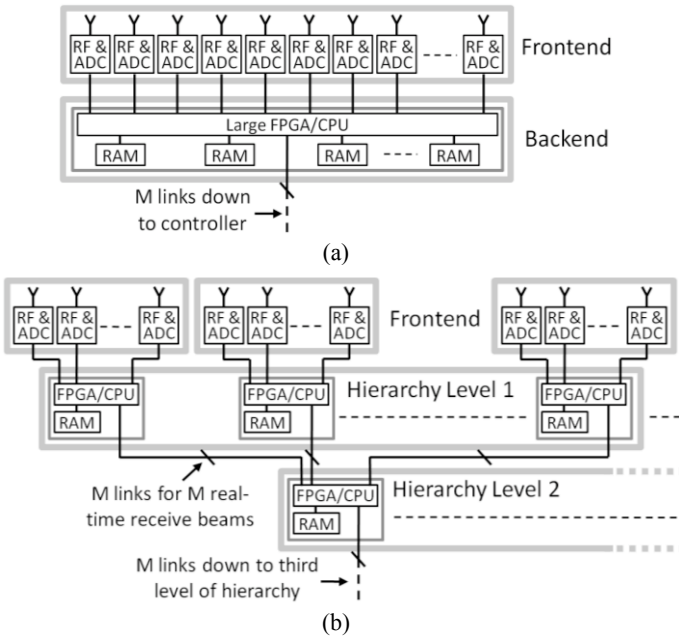

Fig. 3. Digital backend architectures: (a) single-node architecture and (b) hierarchical digital backend

The communication between each quadrant and the control FPGA consists of a low-speed system for commands and data streaming and a high-speed communication system providing a single, real-time data stream at 576 Mbps, the latter consisting of the output of each quadrant FPGA's digital beamformer. A general hierarchical backend would have M real-time data

streams going into each node, allowing for M real-time receive beams. Thus, it has the same multi-beam/volume scan capabilities as a single-node (non-hierarchical) system with the same M streams off its final beamformer output, given that the same processor is used at the base of the hierarchy.

The hierarchical architecture also greatly benefits from processing and data storage at the nodes closest to the elements. Data storage at each element provides the flexibility that allows a multitude of algorithms to be used on the same system simultaneously by streaming this data to the base of the hierarchy when it is needed, even though the total data width to the final processor is limited to M real-time links. For example, one of the M links could be sacrificed in order to stream the raw, element-level data needed to perform adaptive jammer suppression on a periodic basis. This can also aid significantly in calibration and alignment routines, where all transmit/receive channels can be both simultaneously and individually analyzed. Subsequently, the processing at each element could apply calibration weights or even channel equalization. Additionally, processing at each element allows for time-gating and pulse compression (matched filtering), which can significantly decrease the overall amount of data that needs to be sent and analyzed in certain radar applications. These ideas are each demonstrated in the next section through an indoor target tracking example using the DAR prototype.

III. Target Tracking with Hierarchical Techniques

A. Description and Implementation of Procedure

An indoor target tracking procedure is presented here to demonstrate the functionality of the DAR prototype as a full radar system and to illustrate the benefits of a hierarchical digital backend with full element control. The end goal is to track the return (scattered) signal strength and angular location of a small target in an indoor/cluttered environment. The radar does this by turning the DAR into a bi-static array, as illustrated in Fig. 4. The bottom two elements use FPGA-based direct digital synthesizers to transmit 14 MHz wide, 10 µs linear frequency modulated (LFM) waveforms that are upconverted to 3.3 GHz, and the top two rows of elements receive them. Clutter and mutual coupling terms are digitally removed from the received data, and a monopulse comparison test is performed on the demodulated (match-filtered) output peaks to determine the angle of the target. The result is used to update the scanning angle in the system; in this manner, the target is tracked. The steps involved in successfully implementing this are described below.

The first thing that must be done for the radar to function properly is to calibrate and align the transmitters and the receivers. Any direct-conversion transceiver is prone to small I/Q gain/phase and DC offset/LO feedthrough issues [6], which degrade the signal integrity. These can be counteracted through the application of small digital corrections to the raw

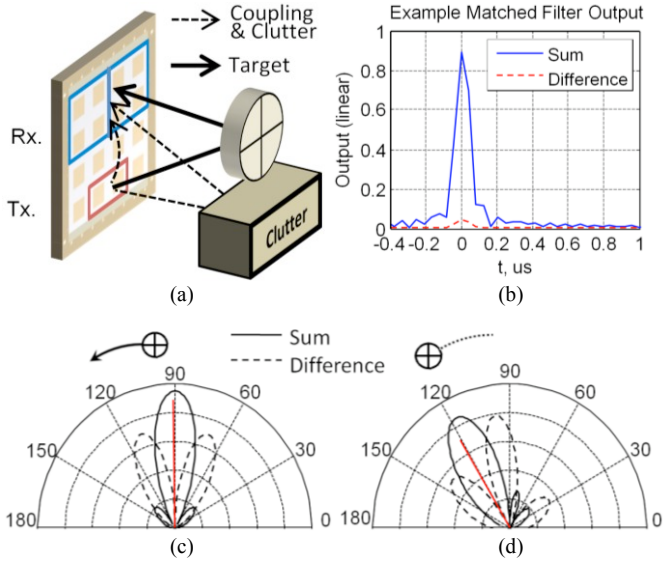

Fig. 4. Indoor target tracking illustration. (a) bi-static radar setup in cluttered environment, (b) example LFM demodulation, (c) tracking a target at broadside (90º), (d) target is tracked out to 120º.

data. On transmit, this is aided enormously by the fact that the DAR prototype has an individually-programmable DDS at each element, where small corrections can be made to improve transmitter spurs.

The receiver uses the ability of the hierarchical digital beamformer to periodically stream raw element-level data to the host PC for the purpose of quadrature calibration *and* automatic element-to-element alignment of amplitude and phase. This is enabled because, unlike some traditional digital radars, all element-level data is *always* stored, and it is only streamed when needed. Presently, the DAR prototype implements the following general linear transformation on the quadrant FPGAs to simultaneously correct for quadrature imbalanace while aligning and weighting each element:

$$\begin{bmatrix} I' \\ Q' \end{bmatrix} = \begin{bmatrix} C_{11} & C_{12} \\ C_{21} & C_{22} \end{bmatrix} \begin{bmatrix} I - I_{DC} \\ Q - Q_{DC} \end{bmatrix} \qquad (1)$$

A broadside transmit CW source is presented to the array and, with the single press of a button, the raw data is streamed and the coefficients in (1) are calculated and sent to the quadrant FPGAs, resulting in automatic calibration and alignment of the array. For wideband applications, a digital filter could be implemented at each element to equalize and time-delay the channel over a wide frequency range, as in [7]. The ability of the this technique to reduce receiver spurs is shown in Fig. 5, where the DC offset can be reduced to more than 50 dB below the 16-element sum's main tone, and the spur due to I/Q imbalance can be pushed down below 60 dB using only 50 µs of raw data.

Another process that must be completed for the tracking to work is to accurately characterize and remove the mutual coupling and clutter reflections of the transmitted waveform in

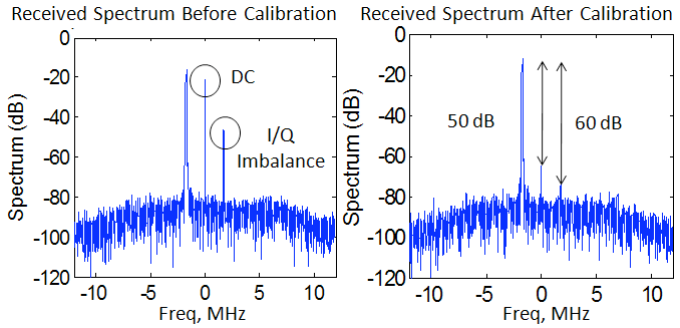

Fig. 5. Reduction in I/Q imbalance spurs on receive array through automatic quadriture calibration.

order to detect the target. Again, the hierarchical digital beamformer with element-level control allows for this. Not only does the element-level control permit simultaneous bi-static operation (where only two elements are transmitting with the rest receiving), but it has the inherent ability to quantify the element-level mutual coupling and clutter reflection when no target is present by streaming the raw element data to a host PC with the bottom two elements transmitting their LFM waveforms. Once this is done, the system can compensate for the mutual coupling and clutter when the target is present by calculating and subtracting off these terms from the overall sum and difference beams obtained through the main digital beamformer since the system knows its own element-level transmit and receive weights. In this manner, the DAR prototype demonstrates how the hierarchical backend is flexible enough to enable clutter/jammer suppression operations that only periodically require element-level data.

The final aspect of the target tracking process is to receive the sum and difference beams through the main link. When this is done in the demonstration, the data is actually time-gated so that only the time-domain data corresponding to the target (from the start of the pulse to a few samples beyond the end of the pulse) is streamed back. Thus, only a small amount of data from the receive beams actually needs to be streamed out to be demodulated. Element-level pulse compression could even further reduce the amount of data.

The result of a test run of the target tracking done inside a typical office room using a small retro-reflector is shown in Fig. 6. As the retro-reflector moves across the room, the error in angle tracking varies as the multipath interference and overall effective radar cross section vary. However, the error is only significant (above 2 degrees) when the ratio of the target's return strength to the overall mutual coupling and clutter contribution to each element is approaching the limits imposed by the dynamic range and phase noise of the system.

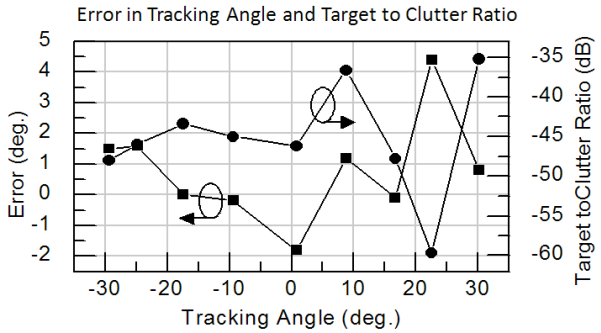

Fig. 6. Error in angluar measurement of indoor target along with the ratio of the target to clutter and mutual coupling strength

IV. Conclusion

As phased-array radar systems continue to evolve with increases in the levels of integration and the role of digitization, new architectures and physical realizations are becoming both possible and necessary. We have presented a prototype of a system that embraces the concept of low-cost integration while demonstrating the viability and benefits of using a hierarchical digital backend; this provides a solution to the problem of how to manage digital data in an intelligent manner while still offering full radar functionality. This was demonstrated by examining the role of the hierarchical digital backend in enabling an indoor, bi-static monopulse target tracking in an efficient manner.

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